6000 Teutonia Avenue, Milwaukee, WI 53209 USA
Tel: (800) 231-8327 (414) 438-3850 Fax: (414) 438-4234
email: techservice@sial.com sigma-aldrich.com

Product Information

6,13-Bis(triisopropylsilylethynyl)pentacene

Catalog Number **716006**
Store at Room Temperature
Technical Bulletin AL-269

TECHNICAL BULLETIN

CAS RN 373596-08-8
Synonym: TIPS-Pentacene

Product Description
With the discovery of organic semiconductors more than twenty years ago, researchers have constantly sought materials with superior performance and a lower cost of processing. Soluble semiconductors are a key part of developing low-cost circuits and flexible circuit design, enabling all-additive processing (single step for deposition and patterning) and eliminating the need for expensive subtractive steps involving traditional photolithography.

One of the best known and highest performing small-molecule organic semiconductors is TIPS-Pentacene. TIPS-Pentacene is soluble in a wide range of solvents and does not require a thermal conversion after deposition. It is also stable in air allowing easy handling without an inert atmosphere. With these benefits, it is critical to understand how to maximize the potential for TIPS-Pentacene and how it might be used in a wide variety of electronic applications and processes.

Precautions and Disclaimer
This product is for R&D use only, not for drug, household, or other uses. Please consult the Material Safety Data Sheet for information regarding hazards and safe handling practices.

Preparation Instructions
Coating Solution – prepare a solution containing ~3.4 wt.% PVP and 1.1 wt.% poly(melamine-co-formaldehyde) (Catalog Number 418560) in PGMEA solvent (Catalog Number 484431)

Semiconductor Solution – prepare a solution consisting of 2 wt.% TIPS-Pentacene (Catalog Number 716006) dissolved in a solvent blend consisting of 91% anisole (Catalog Number 296295) and 9% decane (Catalog Number 457116) by weight.

Storage/Stability
Store the product at room temperature.

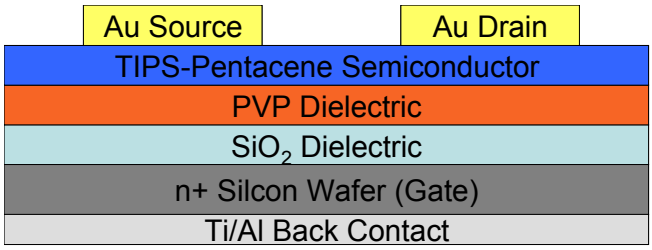
Procedure
As with all semiconductors, there are a number of critical parameters necessary to obtain the optimal performance of TIPS-Pentacene. Among other variables, these parameters include:

- complimentary choices in solvent
- deposition method
- drying method
- contact treatments
- dielectric material
- contact metal

With the right combination of parameters, TIPS-Pentacene has been demonstrated to achieve some of the highest mobility (up to 1.8 cm^2/Vs)[1] and performance results in the industry to date.

Fabrication
The TIPS-pentacene semiconductor can be applied in a very straightforward procedure using a dip coating method. Whereas specific procedures for specific devices will need to be developed by each scientist or engineer, this bulletin presents starting guidelines. For the sake of simplicity, a bottom gate thin film transistor (TFT) device is used as the example (see Figure 1). With this dip process, TIPS-Pentacene should lead to excellent device performance, as well as consistent and repeatable results.

Figure 1.
Cross-section of TIPS-Pentacene thin-film transistor



1. Start with a heavily doped n-type silicon wafer (As) with 1,000 Å of thermal oxide on the front surface and coated with 100 Å titanium nitride and 5,000 Å aluminum on the back.

2. Deposit a layer of poly(4-vinylphenol) (PVP, (Catalog Number 436216) ~100 nm thick by spin coating the Coating Solution at 2,000 rpm.

3. Place the sample on a hotplate for 2 minutes at 100 °C to evaporate the PGMEA followed by 30 minutes at 160 °C to effect the cure.

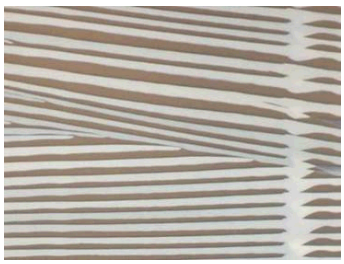
4. Filter the Semiconductor Solution through a 0.2 μm PTFE filter (Catalog Number Z134171 or Z134201) prior to use.

5. Use ~5 mL of Semiconductor Solution to fill the dip coating reservoir. This volume requires ~100 mg of semiconductor sample.

6. Coat the semiconductor solution using a draw rate of 3–5 millimeters per minute using a vertical dip coating apparatus (e.g., NIMA D1L).

7. After coating allow the sample to dry at room temperature under atmospheric conditions. This dip coating method results in the formation of long crystals on the dielectric surface, typically oriented parallel to the dip axis (see Figure 2**)**.

Figure 2.
TIPS-Pentacene film formed by dip coating



8. Deposit gold source and drain electrodes (800–1,000 Å thick) via thermal evaporation through a shadow mask. Orient the source and drain contacts such that the direction of current flow is parallel to the dip coating axis, therefore, along the long axis of the crystals.

9. In this example the channel width and length were 1000 μm and 100 μm, respectively. A cross-section of the device is shown in Figure 1.

Results

Calculations of hole mobility

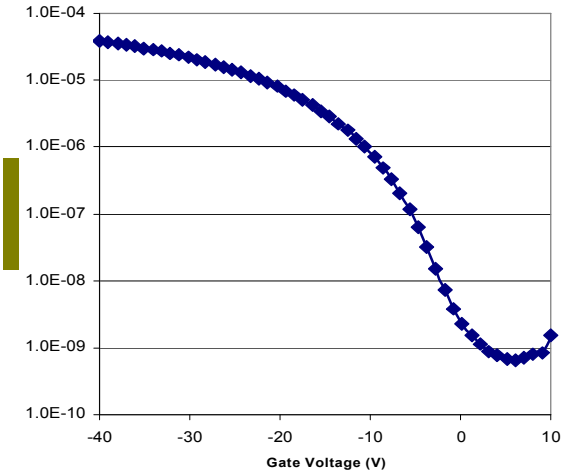
1. The hole mobility (μ) can be calculated from the slope (m) of the plot of the square root of drain current versus V_{GS} using the following equation:

$$\mu = 2\left(\frac{m^2 L}{WC}\right)$$

C is the specific capacitance of the gate dielectric
W is the effective channel width
L is the channel length

Measured mobility values are typically 0.3–0.4 cm^2/Vs using this process, and on/off ratios are typically greater than 10^4. A typical I_D-V_{GS} plot is shown in Figure 3.

Figure 3.
Typical I_D-V_{GS} transfer curve for a dip coated TIPS-Pentacene TFT



2. Alternatively, the mobility can be calculated using the standard equation for drain current in a MOSFET:

$$I_D = \frac{1}{2}\mu C \frac{W}{L}(V_{GS} - V_T)^2$$

The threshold voltage (V_T) is estimated by extrapolating the linear portion of the square root of drain current versus V_{GS} curve back to the x-axis.

If you have any additional questions, please contact Sigma-Aldrich Technical Service:
email: techserv@sial.com
Phone (US Only): 800-231-8327

Reference

1. Park, S.K. et al., Appl.Phys. Lett., **91**, 063514 (2007).

TIPS-Pentacene is a product of 3M and this bulletin was developed in cooperation with the 3M Corporation.

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